Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-218 (canceled)

219. (currently amended) A chip package comprising:

a substrate ~~comprising semiconductor material~~;

only one die having a first top surface at a horizontal level;

an adhesive material joining said substrate and said only one die;

a first insulating layer over said horizontal level, over said only one die, over said substrate and across an edge of said only one die, wherein said first insulating layer comprises ~~comprising~~ a first portion over said only one die and a second portion over said substrate but not over said only one die; ~~, wherein said first insulating layer comprises polyimide; and~~

a ~~first~~ patterned circuit layer over said first insulating layer, over said horizontal level, over said only one die and over said substrate, wherein said patterned circuit layer is connected to said only one die through a first opening in said first insulating layer; ~~.~~

an inductor over said horizontal level and over said first insulating layer; and

a second insulating layer on said inductor.

220. (currently amended) The chip package in claim 219, wherein said only one die comprises a first trace formed therein, and wherein said ~~first~~ patterned circuit layer comprises a second trace having a thickness greater than that of said first trace.

221. (currently amended) The chip package in claim 219, wherein said ~~first~~ patterned

circuit layer comprises a power bus.

222. (currently amended) The chip package in claim 219, wherein said ~~first~~ patterned circuit layer comprises a ground bus.

223. (currently amended) The chip package in claim 219, wherein said ~~first~~ patterned circuit layer connects multiple portions of said only one die through said first opening and through a second opening in said first insulating layer.

Claims 224-227 (canceled)

228. (currently amended) The chip package in claim 219, wherein said first insulating layer comprises polyimide. ~~further comprising a second insulating layer over said first patterned circuit layer.~~

Claims 229-231 (canceled)

232. (currently amended) The chip package in claim 219, wherein said first insulating layer comprises benzocyclobutene (BCB). ~~further comprising a second insulating layer on said first patterned circuit layer, and a second patterned circuit layer on said second insulating layer.~~

Claims 233-235 (canceled)

236. (currently amended) The chip package in claim 219, wherein said adhesive material comprises a conductive paste joining said substrate and said only one die. ~~further comprising a capacitor over said first insulating layer.~~

Claim 337 (canceled)

238. (currently amended) The chip package of claim 219, wherein said adhesive material comprises an adhesive tape joining said substrate and said only one die. ~~further comprising an inductor over said first insulating layer.~~

239. (currently amended) The chip package of claim 219, wherein said patterned circuit layer comprises an electroplated metal. ~~further comprising a resistor over said first insulating layer.~~

240. (currently amended) The chip package of claim 219, wherein said patterned circuit layer comprises a sputtered metal. ~~further comprising a filter over said first insulating layer.~~

241. (currently amended) The chip package of claim 219, wherein said inductor has a portion directly over said substrate but not directly over said only one die. ~~further comprising a wave guide over said first insulating layer.~~

242. (currently amended) The chip package of claim 219 further comprising a metal bump having a portion directly over said substrate but not directly over said only one die. ~~micro electronic mechanic element over said first insulating layer.~~

Claims 243-249 (canceled)

250. (currently amended) The chip package of claim 219, wherein ~~an~~ a second opening in said substrate accommodates said only one die.

251. (currently amended) The chip package of claim 250, wherein said substrate ~~only one die~~ has a second top surface substantially coplanar with said first top surface. ~~that of said substrate.~~

252. (currently amended) The chip package of claim 219, wherein said substrate comprises a first layer and a second layer on said first layer, ~~said first layer being on said second layer, an~~ wherein a second opening in said first layer is over ~~exposing~~ said second layer and accommodates ~~accommodating~~ said only one die.

253. (currently amended) The chip package of claim 252, wherein said second ~~first~~ layer comprises silicon. ~~a semiconductor material.~~

254. (currently amended) The chip package of claim 252, wherein said first layer comprises metal. ~~silicon.~~

255. (currently amended) The chip package of claim 252, wherein said second layer has a material different from that of said first layer. ~~comprises metal.~~

256. (currently amended) The chip package of claim 252, wherein said second layer ~~only one die~~ has a second top surface substantially coplanar with ~~that of~~ said first top surface and a bottom surface facing said first layer. ~~layer.~~

257. (currently amended) The chip package of claim 219 further comprising a polymer layer on ~~over~~ said substrate, wherein a second opening in said polymer layer is over said substrate and accommodates said only one die. ~~and around said only one die.~~

Claim 258 (canceled)

259. (previously presented) The chip package of claim 257, wherein said polymer layer comprises epoxy.

260. (currently amended) The chip package of claim 219 further comprising a solder bump over said horizontal level. ~~first patterned circuit layer.~~

Claim 261 (canceled)

262. (currently amended) The chip package of claim 219 ~~260~~ further comprising a gold bump over said horizontal level. ~~first patterned circuit layer.~~

263. (currently amended) The chip package in claim 219, wherein said only one die comprises multiple active devices, and said ~~first~~ patterned circuit layer connects said multiple active devices through said first opening and through a second opening in said first insulating layer.

264. (previously presented) The chip package in claim 219, wherein said substrate comprises silicon.

265. (currently amended) The chip package in claim 219, wherein said ~~first~~ patterned circuit layer comprises copper.

266. (currently amended) The chip package in claim 219, wherein said substrate comprises metal. ~~first patterned circuit layer is connected to said only one die through an opening in said first insulating layer.~~

267. (currently amended) The chip package in claim 219, wherein said inductor comprises copper. ~~first patterned circuit layer over said only one die and across an edge of said only one die.~~